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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,334	11/21/2003	Edmund D. Blackshear	FIS920030315US1	2621

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,334	BLACKSHEAR, EDMUND D.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/21/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/719334 Attorney's Docket #:FIS920030315US1
Filing Date: 11/21/2003;

Applicant: Blackshear

Examiner: Alexander Williams

Applicant's Status Inquiry Request filed 7/5/05 has been acknowledged.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: The reference numbers in figure 3 are not clearly identified properly. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The disclosure is objected to because of the following informalities: In the specification on page 8, line 16, "Fig. 2A" is described. However, the is no drawing identifying a figure 2A.

Appropriate correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1 to 15 are rejected under 35 U.S.C. § 102(e) as being anticipated by Akram et al. (U.S. Patent # 6,815,251 B1).

1. Akram et al. (figures 1 to 15) specifically figure 15 show a high density memory card comprising: a module card **10** on which there are assembled a plurality of dual device stacks **12A,12B,14A,14B,14C** each having a center bus wire **44**, said plurality of dual device stacks including: a first lower layer memory device **14A-C** attached to a substrate **20**, said substrate having a plurality of wire bond pads adjacent to an aperture **30A,30B,30C** in said substrate center for connection to said center bus wire; and a first upper layer memory device stacked on top of said first lower layer memory device such that said first upper layer memory device is offset over said first lower layer memory device exposing said center bus wire of said first upper layer memory device to some of said plurality of wire bond pads **22** at an edge of said first lower layer memory device; said center bus wire of said upper layer memory device connected to said wire bond pads of said substrate around said edge of said first lower layer memory device.

2. The memory card of claim 1, Akram et al. show including said substrate having apertures therethrough such that said center bus wire of said upper, layer memory device traverses through said aperture to said wire bond pads on the opposite side of said substrate from that which said lower layer memory device is bonded.

3. The memory card of claim 1, Akram et al. further including said dual device stacks placed adjacent to one another in a line.

4. The memory card of claim 3, Akram et al. show wherein said dual device stacks are placed in an array comprising rows and columns.
5. The memory card of claim I, Akram et al. show wherein said offset further includes placing an end of an upper layer memory device of a first dual device stack at approximately the center of a lower layer memory device of a second dual device stack.
6. The memory card of claim 1, Akram et al. show wherein said lower layer memory device attaches to said module card via ball grid arrays **50**.
7. Akram et al. (figures 1 to 15) specifically figure 15 show a substrate **20** having wire bond pads and a plurality of memory devices **12A,12B,14A-C** with center bus wires **44** attached thereto, said substrate comprising: a first layer of said plurality of memory devices **12A,12B** attached to said wire bond pads, adjusted such that a gap exists between adjacent first layer memory devices; and a second layer of said plurality of memory devices **14A-C**, each second layer device bonded to and on top of a first layer device such that said center bus wire of said second layer device traverses through said gap to said wire bond pads.
8. The substrate of claim 7, Akram et al. further comprising said substrate having apertures **30A-C** therethrough such that said center bus wires of said second layer devices traverse through said apertures to wire bond pads on the opposite side of said substrate from that which said first layer memory devices are bonded.
9. The substrate of claim 7, Akram et al. show wherein each of second layer devices is offset from said first layer devices underneath by approximately a device width, such that each of said second layer devices is centered with respect to said gaps.
10. Akram et al. (figures 1 to 15) specifically figure 15 show a method of assembling memory devices **12A,14A** having center bus wires, said method comprising: providing a substrate **20** having a top and bottom surface with wire bond pads for electrical connection; bonding a first dual device stack of memory devices **12A,12B,14A-C** having an upper memory device and a lower memory device to said wire bonds on said top surface of said substrate, said lower memory device placed adjacent to a lower memory device of a second dual device stack of memory devices **12B,14B**, with gaps therebetween; and bonding a second dual device stack of memory devices to said first

dual device stack of memory devices such that an upper memory device in said second dual device stack of memory devices is offset over said gap with said center bus wires traversing therethrough.

11. The method of claim 10, Akram et al. further comprising having said center bus wire of said upper memory device traverse through an aperture in said substrate to electrically connect with said wire bond pads cm said substrate's bottom side.

12. The method of claim 10, Akram et al. includes having said offset adjusted for approximately centering each of said upper memory devices of said dual device stack of memory devices over two adjacent lower memory devices of said dual device stack of memory devices.

13. The method of claim 10, Akram et al. includes placing said dual device stacks of memory devices adjacent to one another in a line.

14. The method of claim 13, Akram et al. show wherein placing said dual device stacks of memory devices includes forming an array of said dual device stacks of memory devices comprising rows and columns.

15. The method of claim 10, Akram et al. includes encapsulating **40** some of said dual device stacks in resin on a portion of surfaces or all surfaces.

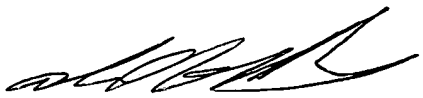
The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/679,680,686,685,723,777,778,673,676,666,774,773,728,724,725,784,786,691,696,698,358 361/716,719,767,782,783,737,738,782	9/12/05
Other Documentation: foreign patents and literature in 257/679,680,686,685,723,777,778,673,676,666,774,773,728,724,725,784,786,691,696,698,358 361/716,719,767,782,783,737,738,782	9/12/05
Electronic data base(s): U.S. Patents	9/12/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
9/12/05